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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ICHIRO FUJIMORI

Appeal 2009-011990
Application 10/801,260[1]
Technology Center 2800

Decided: February 3, 2010

Before ROBERT E. NAPPI, MARC S. HOFF, and THOMAS S. HAHN, *Administrative Patent Judges*.

HOFF, *Administrative Patent Judge*.

DECISION ON APPEAL

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[1] The real party in interest is Broadcom Corporation.

STATEMENT OF CASE

Appellant appeals under 35 U.S.C. § 134(a) from a Final Rejection of claims 1-15. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm-in-part.

Appellant's invention relates to a method for reducing noise in an electronic device. The device comprises a substrate layer, and a transistor layer that is shielded from the substrate layer by a shielding layer. At least one transistor of a first transistor type couples the transistor layer to the shielding layer and a quiet voltage source may be coupled to the transistor of the first transistor type. At least one transistor of a second transistor type is coupled to the shielding layer (Spec. 4).

Claim 1 is exemplary of the claims on appeal:

1. A system for reducing noise in a chip, the system comprising:
a substrate layer integrated within the chip;
a transistor layer integrated within the chip, which is shielded from said substrate layer by a shielding layer, wherein said shielding layer reduces transfer of noise in the chip;
at least one transistor of a first transistor type that couples said transistor layer to said shielding layer; and
a positive potential of a quiet voltage source that is coupled to said at least one transistor of said first transistor type.

The Examiner relies upon the following prior art in rejecting the claims on appeal:

Puar	US 6,356,497 B1	Mar. 12, 2002
McCormack	US 6,395,591 B1	May 28, 2002
Wei	US 6,403,992 B1	Jun. 11, 2002

Claims 1-10, 12, 14, and 15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over McCormack in view of Puar.

Claims 11 and 13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over McCormack in view of Puar and Wei.

Claims 1-13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Wei in view of Puar.[2]

Throughout this decision, we make reference to the Appeal Brief ("App. Br.," filed August 15, 2007), the Reply Brief ("Reply Br.," filed January 14, 2008), and the Examiner's Answer ("Ans.," mailed November 15, 2007) for their respective details.

ISSUES

With respect to the rejection over McCormack in view of Puar, Appellant argues that McCormack fails to teach a shielding layer that reduces transfer of noise in the chip. Appellant argues that the p-epi layer 12 and substrate layer 10 of McCormack do not possess the resistivity characteristics necessary to cause p-epi layer 12 to reduce transfer of noise (App. Br. 6-10).

With respect to the rejection over Wei in view of Puar, Appellant argues that Wei does not disclose or suggest any transistor that couples a transistor layer with the shielding layer (App. Br. 25). Appellant further argues that Wei does not teach a transistor resistively, or capacitively, coupled to the shielding layer, as required by dependent claims (App. Br. 26-27).

[2] In the Examiner's Answer, the Examiner has withdrawn the rejection of claims 1, 8, 9, 12, 14, and 15 under § 103 as being unpatentable over Puar in view of McCormack.

Appellant's contentions present us with the following issues:

1. Has Appellant shown that the Examiner erred in finding that McCormack teaches a shielding layer which shields a transistor layer from a substrate layer and reduces transfer of noise?

2. Has Appellant shown that the Examiner erred in finding that Wei teaches at least one transistor of a first transistor type that couples the transistor layer to the shielding layer?

FINDINGS OF FACT

The following Findings of Fact (FF) are shown by a preponderance of the evidence.

The Invention

1. Appellant discloses a PMOS transistor 100 (having body B, source S, and drain D) disposed in N-well 120 (Fig. 2).

2. Appellant's Figure 2 shows NMOS transistor 90 coupled to P-well 110, which is itself coupled to N-well 80.

3. Appellant discloses a P-P junction of P-well 110 and the P+ body (B) of the transistor (Fig. 2).

4. Appellant discloses a P-N junction of N-well 120 and the P+ source (S) of the transistor (Fig. 2).

Wei

5. Wei teaches a PMOS transistor (having body B, source S, and drain D) disposed in an N-well (46). The PMOS transistor is coupled to the N-well (i.e., the transistor layer), which is itself coupled to N-well 484 (Fig. 4).

6. Wei further teaches an NMOS transistor coupled to P-well 46, which is itself coupled to N-well 484 (Fig. 4).

7. Wei teaches a resistive coupling formed by P-P junction of the P-well 46 and p+ body (B3) of the second transistor (Fig. 4).

8. Wei teaches a capacitive coupling formed by P-N junction of the N-well 46 and p+ source (S4) of the first transistor (Fig. 4).

McCormack

9. McCormack teaches that a lightly doped p-substrate is problematic because its high resistance renders an IC susceptible to latchup (col. 1, ll. 19-24)

10. According to McCormack, the way to reduce latchup sensitivity is to lower the resistance of the P-wells (col. 4, ll. 9-13).

11. McCormack teaches that heavy doping of substrates results in low resistivity (col. 1, ll. 25-30).

12. McCormack teaches that substrate 10 is lightly doped and has a resistivity in the range of 14-28 ohm-cm (col. 5, ll. 45-47).

13. McCormack teaches that p-epi layer 12 has a resistivity in the range of 14-28 ohm-cm (col. 6, ll. 1-3).

Puar

14. Puar teaches a graphics controller integrated circuit including a P-channel transistor in an N-type well (Abstract; col. 2, ll. 45-47).

PRINCIPLES OF LAW

On the issue of obviousness, the Supreme Court has stated that "the obviousness analysis cannot be confined by a formalistic conception of the words teaching, suggestion, and motivation." *KSR Int'l Co. v. Teleflex Inc.*,

550 U.S. 398, 419 (2007). Further, the Court stated "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *Id.* at 416. "One of the ways in which a patent's subject matter can be proved obvious is by noting that there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims." *Id.* at 419-420.

Under the doctrine of inherency, if a claimed element is not expressly disclosed in a prior art reference, the reference nevertheless anticipates the claim if the missing element is necessarily present in the reference, and it would be so recognized by skilled artisans. *Rosco, Inc. v. Mirror Lite Co.*, 304 F.3d 1373, 1380 (Fed. Cir. 2002). To anticipate the claim, the missing element must be *necessarily present* in the prior art—not merely probably or possibly present. *Id.*

In re Swinehart, 439 F.2d 210 (CCPA 1971), sets forth the burden of proof required to overcome an inherency rejection:

> [I]t is elementary that the mere recitation of a newly discovered function or property, inherently possessed by things in the prior art, does not cause a claim drawn to those things to distinguish over the prior art. Additionally, where the Patent Office has reason to believe that a functional limitation asserted to be critical for establishing novelty in the claimed subject matter may, in fact, be an inherent characteristic of the prior art, it possesses the authority to require the applicant to prove that the subject matter shown to be in the prior art does not possess the characteristic relied on. [439 F.2d at 212-13, 58 CCPA at 1031, 169 USPQ at 229.] This burden was involved in *In re Ludtke*, 441 F.2d 660, 58 CCPA 1159, 169 USPQ 563 (1971), and is applicable to product and process claims reasonably considered as possessing the allegedly inherent characteristics.

In re Best, 562 F.2d 1252, 1254-55 (CCPA 1977).

ANALYSIS

A. SECTION 103 REJECTIONS OVER MCCORMACK IN VIEW OF PUAR

Claim 1 requires a shielding layer which shields a transistor layer from a substrate layer, wherein the shielding layer "reduces transfer of noise in the chip." The Examiner finds that p-epi layer 12 of McCormack reduces noise because it isolates substrate 10 from transistor layer and it has a higher doping than the underlying substrate (Fin. Rej. 2-3).

Figure 2 of McCormack is reproduced below:

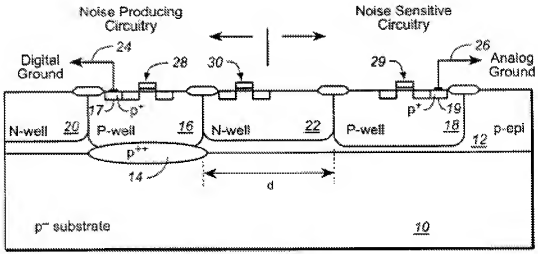

FIG._2

Figure 2 is a cross-sectional view of a CMOS structure.

The Examiner cites to columns 1 and 4 of McCormack, respectively, to establish these two propositions (Fin. Rej. 2-3). We agree with Appellant, however, that the cited sections of McCormack do *not* disclose actual characteristics of layer 12 and substrate 10. McCormack teaches that a lightly doped p-substrate is problematic because its high resistance renders an IC susceptible to latchup (FF 9), and that the way to reduce latchup sensitivity is to lower the resistance of the P-wells (FF 10). McCormack

further teaches that heavy doping of substrates results in low resistivity (FF 11).

McCormack does not specify, however, that p-epi layer 12 and substrate 10 are composed of differentiated materials in such a way that would achieve the shielding and noise reduction disclosed by Appellant. McCormack teaches that substrate 10 is lightly doped and has a resistivity in the range of 14-28 ohm-cm (FF 12). McCormack teaches that p-epi layer 12 (also) has a resistivity in the range of 14-28 ohm-cm (FF 13). Because McCormack teaches that both p-epi layer 12 and substrate 10 have resistivities in the same range, we find that one is not doped more lightly or heavily than the other. Therefore, we find that McCormack does not teach a region of relatively lower resistance that would reduce latchup sensitivity. As a result, we find that McCormack does not teach a shielding layer that reduces transfer of noise, and that Appellant has shown that the Examiner lacks factual support for his conclusion that claim 1 would have been obvious.

Appellant has shown that the Examiner erred in rejecting claim 1 under § 103 as being unpatentable over McCormack in view of Puar. Thus, we will not sustain the rejection of claim 1 or of claims 2-10, 12, 14, and 15, dependent therefrom.

B. SECTION 103 REJECTION OVER WEI IN VIEW OF PUAR

1. CLAIMS 1, 8, AND 13

We select claim 1 as representative of this group of claims, pursuant to our authority under 37 C.F.R. § 41.37(c)(1)(vii).

Appellant argues that the combination of Wei and Puar does not disclose or suggest at least one transistor of a first transistor type that

couples the transistor layer to the shielding layer (App. Br. 24). Appellant contends that Wei does not disclose or suggest any transistor that couples a transistor layer of any of the PMOS or NMOS 46 with the alleged shielding layer 484 (App. Br. 25).

We do not consider Appellant's argument persuasive. Wei Figure 4 teaches, *inter alia*, a PMOS transistor (having body B, source S, and drain D) disposed in an N-well (46). The PMOS transistor is coupled to the N-well (i.e., the transistor layer), which is itself coupled to N-well 484 (FF 5). Figure 4 of Wei is reproduced below:

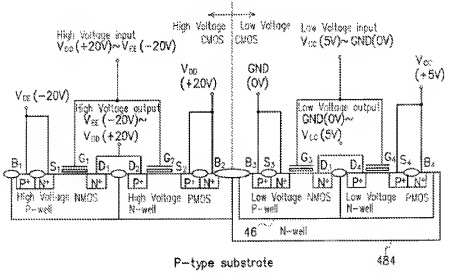

FIG. 4 (PRIOR ART)

Figure 4 is a schematic, cross-sectional view of a conventional CMOS device.

This structure is analogous to the structure illustrated in Appellant's Figure 2, which shows a PMOS transistor 100 (having body B, source S, and drain D) disposed in N-well 120 (i.e., the transistor layer)(FF 1). Wei thus teaches identical structure to that disclosed by Appellant. We therefore find that the PMOS transistor of Wei functions to couple the transistor layer (46)

to the shielding layer (484) in the same manner that Appellant's PMOS transistor couples its transistor layer (120) to its shielding layer (80).

We therefore find no error in the Examiner's rejection of representative claim 1. Accordingly, we will sustain the rejection of claims 1, 8, and 13 under § 103 as unpatentable over Wei in view of Puar.

2. CLAIMS 2-7

We select claim 2 as representative of this group of claims, pursuant to our authority under 37 C.F.R. § 41.37(c)(1)(vii).

Appellant argues that Wei does not disclose a transistor of a second transistor type that is resistively coupled to the shielding layer (App. Br. 26). We do not consider Appellant's argument to be persuasive. First, representative claim 2 merely requires that the transistor of a second type be coupled to the shielding layer. Second, Wei teaches an NMOS transistor coupled to P-well 46, which is itself coupled to N-well 484 (FF 6). Wei's structure is thus identical to that disclosed in Appellant's Figure 2, in which NMOS transistor 90 is coupled to P-well 110, which is itself coupled to N-well 80 (FF 2). We therefore find that Wei teaches the claimed transistor of a second type, coupled to the shielding layer. Third, with respect to the resistive coupling limitation recited in claim 5, the Examiner finds that the resistive coupling disclosed by Appellant (Fig. 2, 180) is formed by P-P junction of P-well 110 and the P+ body (B) of the transistor (Ans. 22; FF 3). The Examiner further finds that, with essentially identical structure, Wei teaches a resistive coupling which is formed by P-P junction of the N-well 46 and p+ body (B3) of the second transistor (Ans. 22; FF 7). Because Wei does not explicitly teach such resistive coupling, we regard the Examiner's position to be that resistive coupling *inherently* occurs as a consequence of

the presence of the P-P junction. Under *In re Best, supra*, that position serves to require an applicant who seeks to rebut it to prove that the subject matter shown to be in the prior art does not possess the characteristic relied on. *Best*, 562 F.2d at 1254-55. Appellant's Reply Brief contains no attempt to rebut the Examiner's finding that resistive coupling is inherent to the P-P junction of P-well 46 and body B3 of the second transistor of Wei, however. Finally, Appellant's argument that resistive coupling 240, rather than resistive coupling 180, is used to couple the transistor to the shielding layer (Reply Br. 22-23) is not persuasive to show Examiner error, because we find that resistive coupling 180 functions to couple transistor 110 to shielding layer 80. The existence of further elements in the coupling "chain" (e.g., capacitive coupling 200) does not negate the existence of such coupling between the transistor and the shielding layer.

We therefore find no error in the Examiner's rejection of representative claim 2. Accordingly, we will sustain the rejection of claims 2-7 under § 103 as unpatentable over Wei in view of Puar.

3. CLAIMS 9-12

We select claim 9 as representative of this group of claims, pursuant to our authority under 37 C.F.R. § 41.37(c)(1)(vii).

Appellant argues that Wei does not disclose a transistor of a first transistor type that is capacitively coupled to the shielding layer (App. Br. 27).

We do not consider Appellant's argument to be persuasive. First, Claim 9 merely recites that at least one transistor of the first transistor type is disposed within the transistor layer. Second, Wei teaches a PMOS transistor disposed within N-well 46 (i.e., within the transistor layer). N-well 46 is

surrounded by N-well 484 (the shielding layer), which resides above a P-type substrate (FF 5). Third, with respect to the capacitive coupling limitation recited in claim 10, the Examiner finds that the capacitive coupling disclosed by Appellant (Fig. 2, 220) is formed by P-N junction of N-well 120 and the P+ source (S) of the transistor (Ans. 25; FF 4). The Examiner further finds that, with essentially identical structure, Wei teaches a capacitive coupling which is formed by P-N junction of the N-well 46 and p+ source (S4) of the first transistor (Ans. 25; FF 8). Because Wei does not explicitly teach such capacitive coupling, we regard the Examiner's position to be that capacitive coupling *inherently* occurs as a consequence of the presence of the P-N junction. Under *In re Best, supra*, that position serves to require an applicant who seeks to rebut it to prove that the subject matter shown to be in the prior art does not possess the characteristic relied on. *Best*, 562 F.2d at 1254-55. Appellant's Reply Brief contains no attempt to rebut the Examiner's finding that capacitive coupling is inherent to the P-N junction of P-well 46 and source S4 of the first transistor of Wei, however. Finally, Appellant's argument that capacitive coupling 200, rather than capacitive coupling 220, is used to couple the transistor to the shielding layer (Reply Br. 26-27) is not persuasive to show Examiner error, because we find that capacitive coupling 220 functions to couple transistor 120 to shielding layer 80. The existence of further elements in the coupling "chain" (e.g., resistive coupling 240) does not negate the existence of such coupling between the transistor and the shielding layer.

We therefore find no error in the Examiner's rejection of representative claim 9. Accordingly, we will sustain the rejection of claims 9-12 under § 103 as unpatentable over Wei in view of Puar.

C. SECTION 103 REJECTION OF CLAIMS 11 AND 13 OVER MCCORMACK IN VIEW OF PUAR AND WEI

Appellant argues that the Examiner erred in rejecting claims 11 and 13 over the combination of McCormack, Puar, and Wei (App. Br. 23). Because we affirm the rejection of claims 11 and 13 over Wei in view of Puar, *supra*, we need not reach the merits of this rejection.

CONCLUSIONS OF LAW

1. Appellant has shown that the Examiner erred in finding that McCormack teaches a shielding layer which shields a transistor layer from a substrate layer and reduces transfer of noise.

2. Appellant has not shown that the Examiner erred in finding that Wei teaches at least one transistor of a first transistor type that couples the transistor layer to the shielding layer.

ORDER

The Examiner's rejection of claims 1-13 is affirmed. The Examiner's rejection of claims 14 and 15 is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

ELD

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